



**SCHEMATICS TABLE:**

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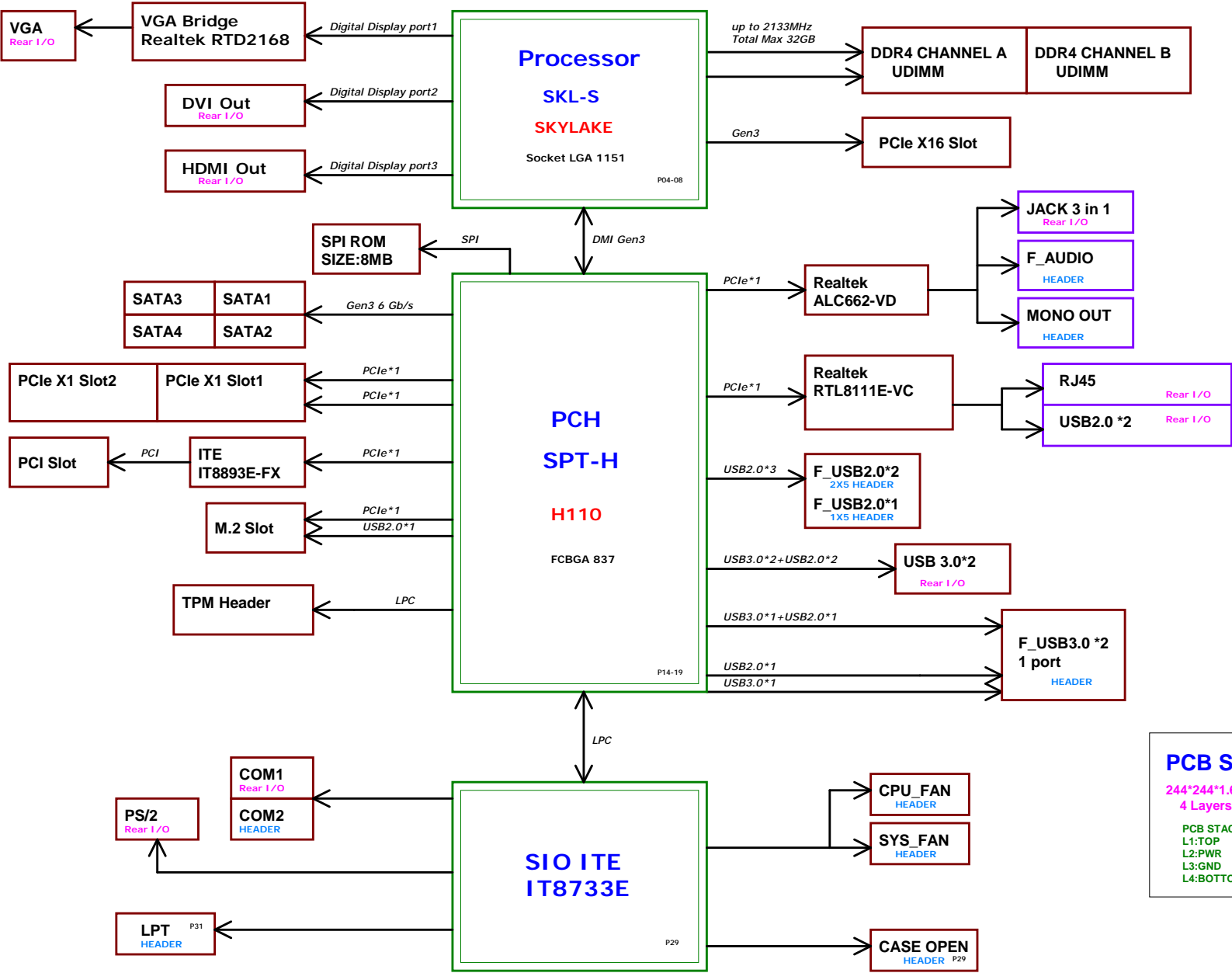
[illegible]

sku	1	2	3	4	5	6	7	8	9	10	11	12	13	14
H110	USB3/PCIe	USB3/PCIe	USB3/PCIe	USB3	N/A	N/A	N/A	N/A	N/A	N/A	N/A	PCIe	PCIe	PCIe
P150	USB3/PCIe	USB3/PCIe	USB3/PCIe	USB3	USB3	USB3	N/A	N/A	N/A	N/A	PCIe	PCIe	PCIe	PCIe
Q150	USB3/PCIe	USB3/PCIe	USB3/PCIe	USB3	USB3	USB3	USB3	USB3	N/A	N/A	PCIe	PCIe	PCIe	PCIe
H170	USB3/PCIe	USB3/PCIe	USB3/PCIe	USB3	USB3	USB3	USB3	USB3	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe
Z170	USB3/PCIe	USB3/PCIe	USB3/PCIe	USB3	USB3	USB3	USB3	USB3	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe
P170	USB3/PCIe	USB3/PCIe	USB3/PCIe	USB3	USB3	USB3	USB3	USB3	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe
Q170	USB3/PCIe	USB3/PCIe	USB3/PCIe	USB3	USB3	USB3	USB3	USB3	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe

26	Pcie #20			X4	X2	Intel® RST for PCIe Storage
25	Pcie #19			X4	X2	Intel® RST for PCIe Storage
24	Pcie #8	SATA #5				
23	Pcie #17	SATA #4				
22	Pcie #6	SATA #3				
21	Pcie #5	SATA #2		X4	X2	Intel® RST for PCIe Storage
20	Pcie #4	SATA #1**			X2	Intel® RST for PCIe Storage
19	Pcie #13	SATA #0**	Gbe			
18	Pcie #12		Gbe		X2	
17	Pcie #11			X4		
16	Pcie #10	SATA #1			X2	
15	Pcie #9	SATA #0	Gbe			

Sku	15	16	17	18	19	20	21	22	23	24	25	26	RST for PCIe Ports
H110	PCIe/ LAN	PCIe	N/A	LAN Only	SAIA*/ LAN	SATA*	SATA	SATA	N/A	N/A	N/A	N/A	
B150	PCIe/LAN SATA*	PCIe/ SATA*	PCIe	PCIe/ LAN	SATA* /LAN	SATA*	SATA	SATA	SATA	SATA	N/A	N/A	
Q150	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	SATA	SATA	SATA	SATA	N/A	N/A	
H170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	SATA	SATA	PCIe	PCIe	
Z170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe	PCIe	
Q170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe	PCIe	

Skylake-S Desktop Platform



**PCB SIZE**  
244\*244\*1.6mm  
4 Layers  
PCB STACK:  
L1:TOP  
L2:PWR  
L3:GND  
L4:BOTTOM

## PCH-GPIO function

Data:2014/10/02

Pin Name	Power Well	Usage	Default Status	Boot Set(BIOS Check)
GPP_A11	3VSB	PME_L	PME#	PME#
GPP_G13	VCC3	HDPANEL_DETECT	GPI	GPI
GPP_G14	VCC3	on-board TPM detect	GPI	GPI
GPP_E7	VCC3	THERMAL_SD	GPI	GPI
GPP_B3	3VSB	BT_DIS_L	GPI	GPO-->Hi
GPP_H15	3VSB	for ACER reserve	GPI	GPI
GPP_H14	3VSB	for ACER reserve	GPI	GPI
GPP_E9	3VSB	BIOS WP Jumper	GPI	GPI
GPP_F16	3VSB	USB_EN	GPI	GPO-->Hi
GPP_F17	3VSB	LPC_PME_L	GPI	GPI
GPP_E0	VCC3	OBR	GPI	GPI
GPD11	DSW	LAN_DIS_L	LANPHYPC	LANPHYPC
GPD9	DSW	PCH_RI_L	SLP_WLAN#	GPI
GPD10	DSW	ME Disable	SLP_S5#	GPO-->Low
GPD0	DSW	RLAN_PWR_EN	BATLOW#	GPO-->Hi
GPP_F22	VCC3	PCH_GPP_F22	GPI	PCH_GPP_F22
GPP_G22	VCC3	TP_VGA	GPI	TP_VGA
GPP_B6	VCC3	CLK_REQ1_M.2_WLAN_L	GPI	CLK_REQ1_M.2_WLAN_L
GPP_B17	3VSB	M.2_DIS_L_R	GPI	M.2_DIS_L_R

## SIO-GPIO function

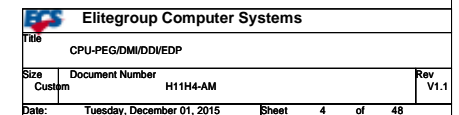
Data:2013/10/01

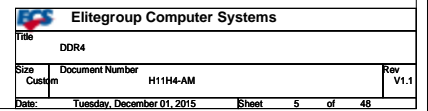
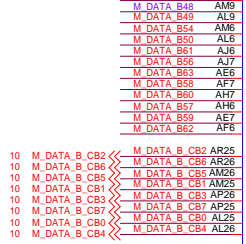
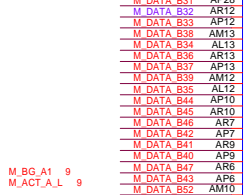
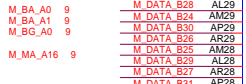
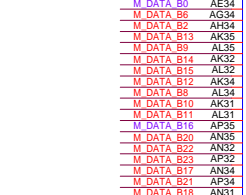
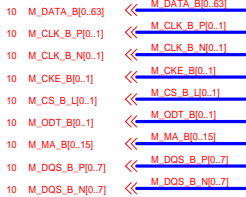
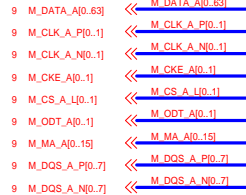
Pin Name	Power Well	Usage	Default SET
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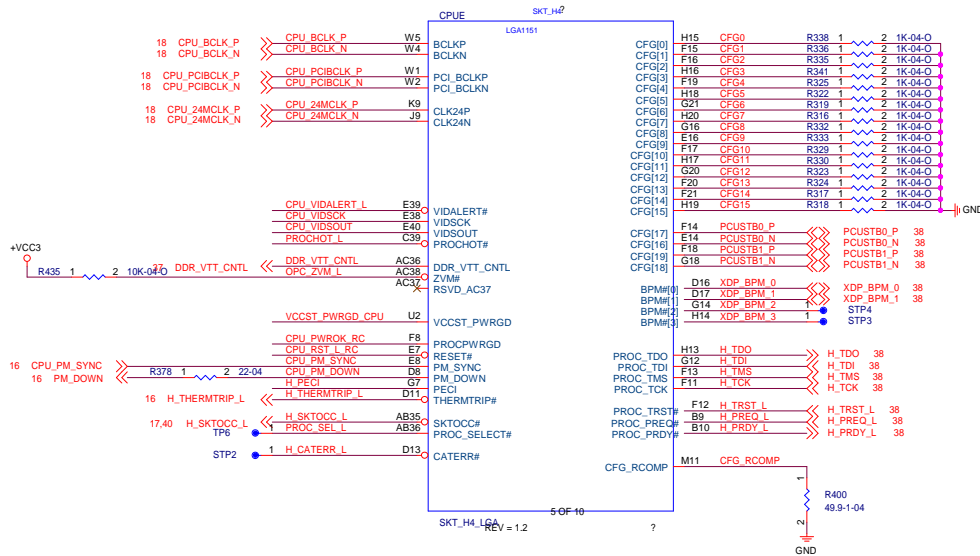
## Interrupt mapping

Data:2014/11/10

Function	INT# port	PCle*1 port	Device
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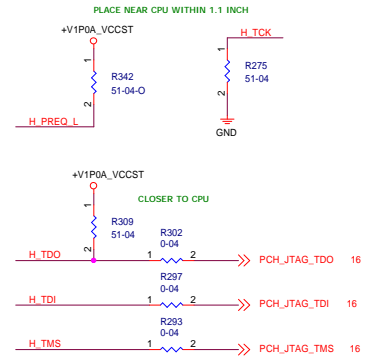






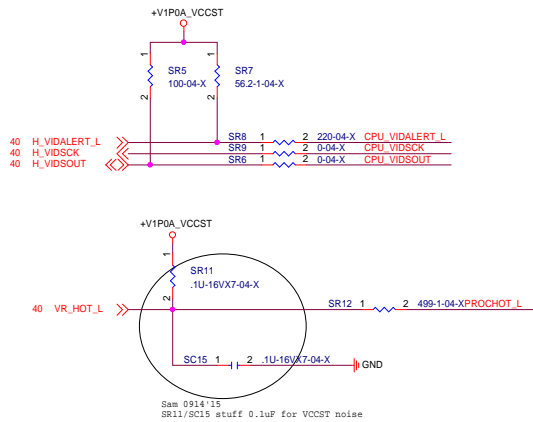
## CFG[0:15] Configuration note

- CFG[0]:** Still not available after CPU PLL lock and core booting.
  - 0 = Configuring Normal Operation; No stall.
  - 0 = Stall.
- CFG[1]:** Reserved configuration item.
- CFG[2]:** PCI Express® Static state Lane Numbering RawSel.
  - 0 = Same operation.
  - 0 = Lane numbers reversed.
- CFG[3]:** Reserved configuration item.
- CFG[4]:** JDF enable.
  - 0 = Disabled.
  - 0 = Enabled.
- CFG[5]:** PCI Express® BPX enable.
  - 0 = 1 x16, 2 x4 PCI Express® reserved.
  - 0 = 2 x16 PCI Express® reserved.
  - 0 = 8 x16 PCI Express® reserved.
- CFG[7]:** PECI settings.
  - 0 = Configured PECI Train immediately following RESET# deassertion.
  - 0 = PECI Wait for 30CS for training.
- CFG[19:8]:** Reserved configuration items.

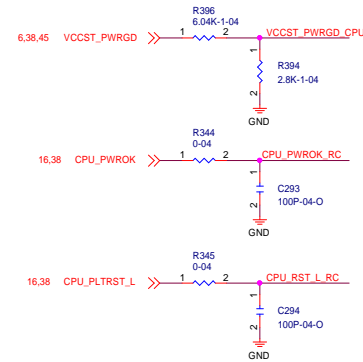


## Sequencing Circuit

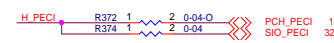
## Asynchronous & Sideband Signal



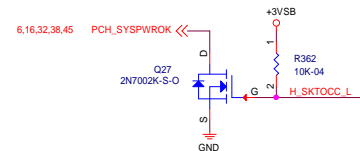
## Processor Power Good



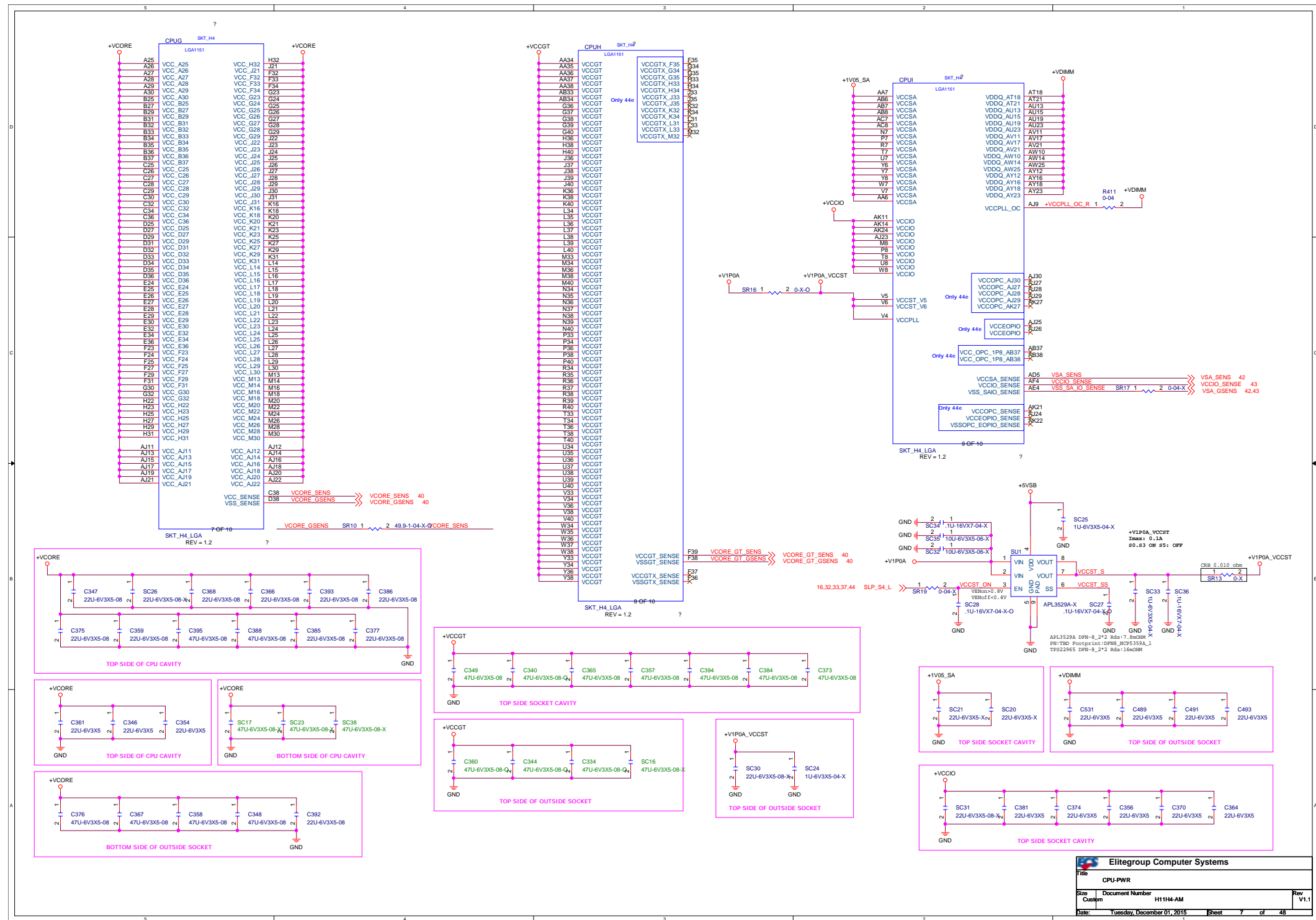
## PECI

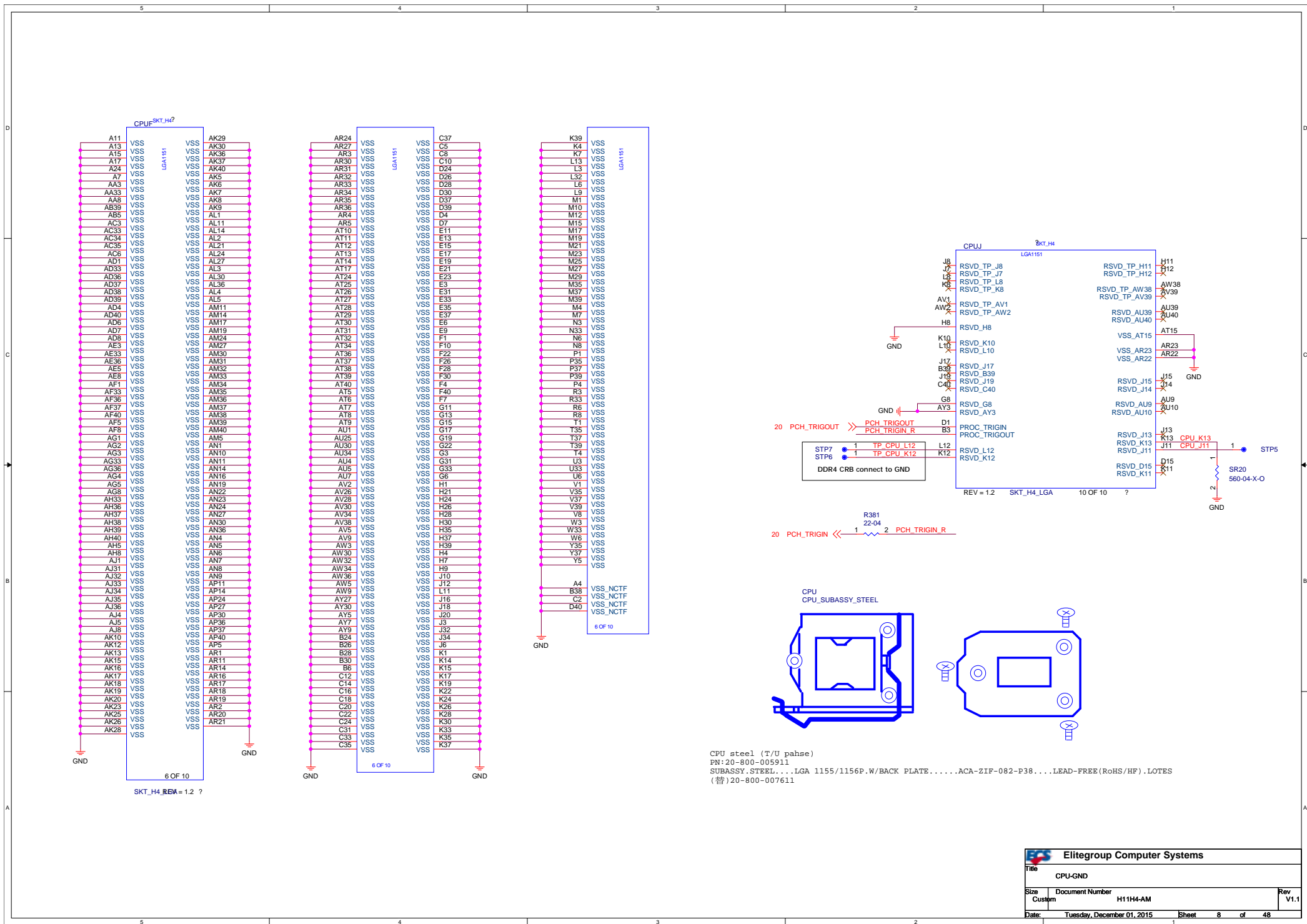


## SKTOCC#



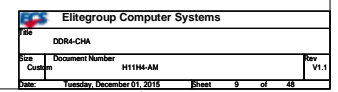


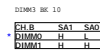




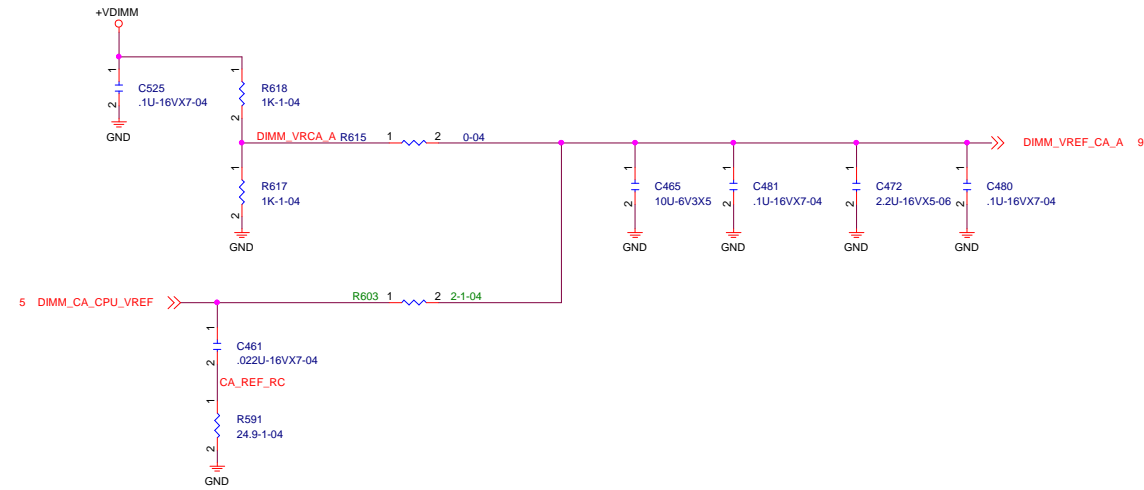
CPU steel (T/U pahse)  
PN:20-800-005911  
SUBASSY.STEEL...LGA 1155/1156P.W/BACK PLATE.....ACA-ZIF-082-P38....LEAD-FREE (RoHS/HP).LOTES  
(替)20-800-007611



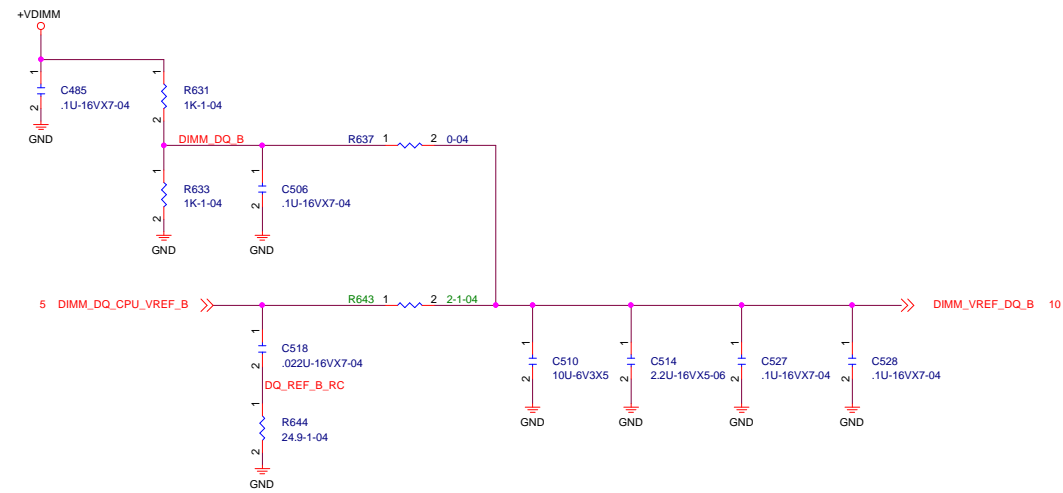




## DIMM\_VREF\_CA



## DIMM\_VREF\_DQ

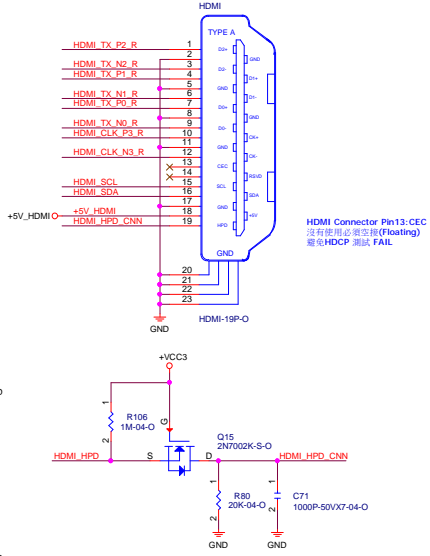
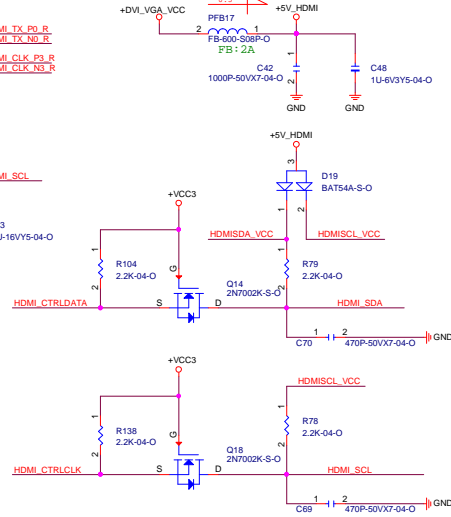
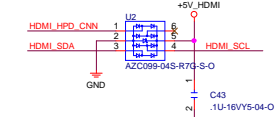
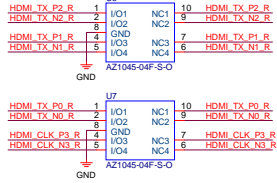
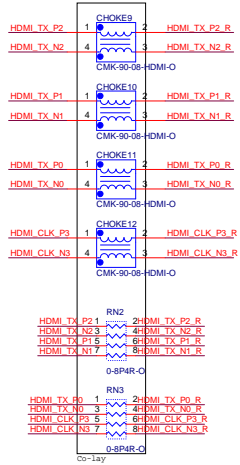
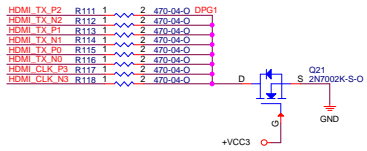


Pin	Signal	Pin	Signal	Pin	Signal
1	DVI TX P2	11	DVI TX P0	21	DVI TX P2
2	DVI TX N2	12	DVI TX N0	22	DVI TX N2
3	DVI TX P1	13	DVI TX P0	23	DVI TX P1
4	DVI TX N1	14	DVI TX N0	24	DVI TX N1
5	DVI TX P0	15	DVI TX P0	25	DVI TX P0
6	DVI TX N0	16	DVI TX N0	26	DVI TX N0
7	DVI TX P3	17	DVI TX P3	27	DVI TX P3
8	DVI TX N3	18	DVI TX N3	28	DVI TX N3

## HDMI

Pin	Signal	Pin	Signal	Pin	Signal
1	DVI TX P2	11	DVI TX P0	21	DVI TX P2
2	DVI TX N2	12	DVI TX N0	22	DVI TX N2
3	DVI TX P1	13	DVI TX P0	23	DVI TX P1
4	DVI TX N1	14	DVI TX N0	24	DVI TX N1
5	DVI TX P0	15	DVI TX P0	25	DVI TX P0
6	DVI TX N0	16	DVI TX N0	26	DVI TX N0
7	DVI TX P3	17	DVI TX P3	27	DVI TX P3
8	DVI TX N3	18	DVI TX N3	28	DVI TX N3

17	HDMI_CTRLCLK	HDMI_CTRLCLK
17	HDMI_CTRLDATA	HDMI_CTRLDATA
17	HDMI_HPD	HDMI_HPD

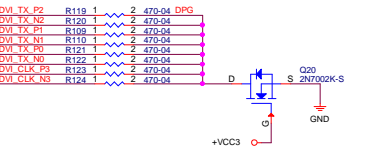


HDMI Connector Pin13: CEC  
沒有使用必置空接(Floating)  
避免HDCP 測試 FAIL

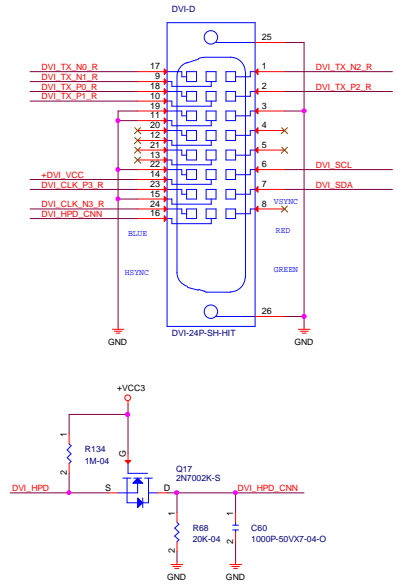
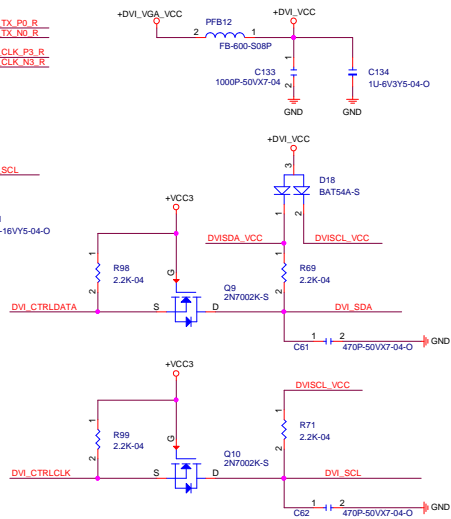
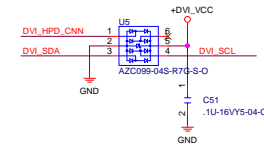
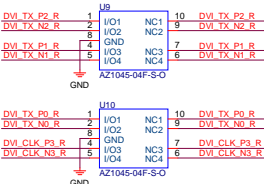
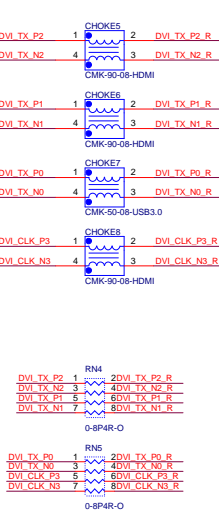
## DVI

Pin	Signal	Pin	Signal	Pin	Signal
1	DVI TX P2	11	DVI TX P0	21	DVI TX P2
2	DVI TX N2	12	DVI TX N0	22	DVI TX N2
3	DVI TX P1	13	DVI TX P0	23	DVI TX P1
4	DVI TX N1	14	DVI TX N0	24	DVI TX N1
5	DVI TX P0	15	DVI TX P0	25	DVI TX P0
6	DVI TX N0	16	DVI TX N0	26	DVI TX N0
7	DVI TX P3	17	DVI TX P3	27	DVI TX P3
8	DVI TX N3	18	DVI TX N3	28	DVI TX N3

17	DVI_CTRLCLK	DVI_CTRLCLK
17	DVI_CTRLDATA	DVI_CTRLDATA
17	DVI_HPD	DVI_HPD

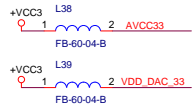


- 16-400-900143 COMMON CHOKE 90 OHM .SMD 0805 .HDMI2012F25P-900T04.400mA...LEAD-FREE(RoHS),TAI-TECH
- 16-400-900171 COMMON CHOKE 90 OHM.25%.SMD 0805 .QTCW2012H-090-LF.300mA...LEAD-FREE(RoHS/HF),MAGIC



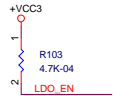
Elitegroup Computer Systems			
Title	DP/HDMI		
Size	Document Number	H1144-AM	Rev
C			V1.1
Date:	Tuesday, December 01, 2015	Sheet	12 of 48

## Power

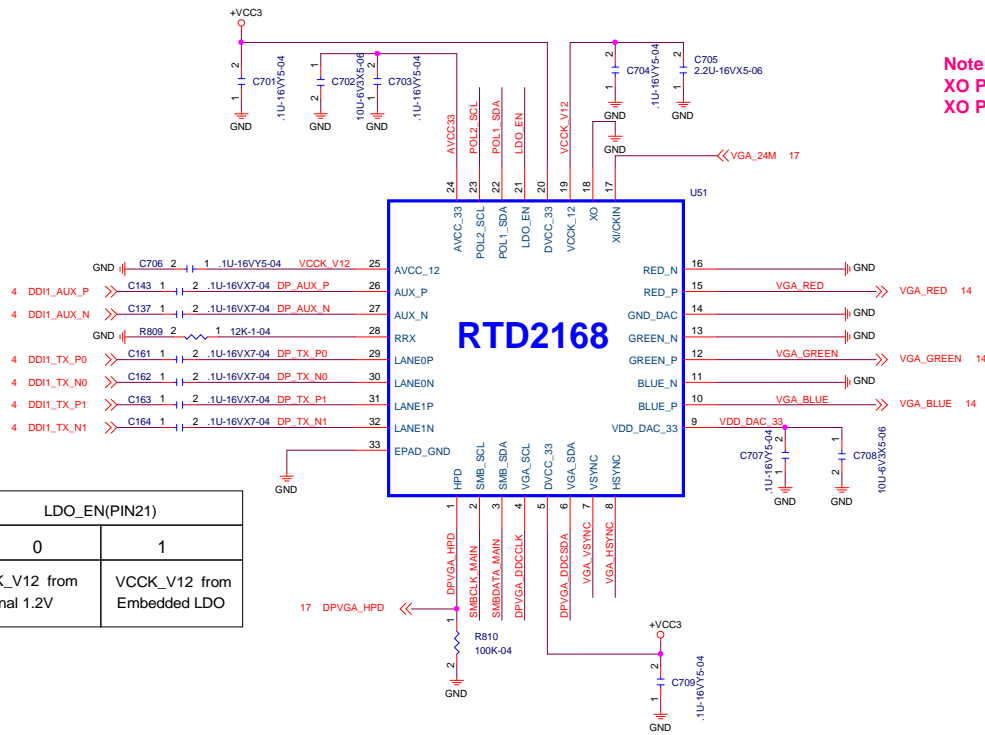


10,16,34,38 SMBDATA\_MAIN  
10,16,34,38 SMBCLK\_MAIN

IIC Protocol is used  
RTD2168 Slave Address:  
0x64/0x65 and 0x68/0x69



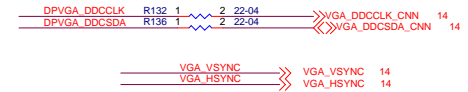
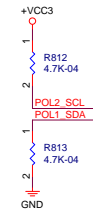
LDO_EN(PIN21)	
0	1
VCCCK_V12 from External 1.2V	VCCCK_V12 from Embedded LDO



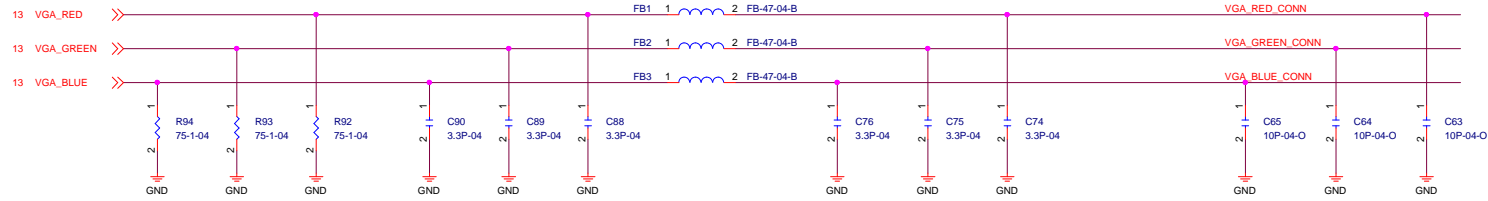
Note: When connected to non-EDID monitor,  
XO Pin Pull Down : Disable RTD2168 embedded EDID, CPU handle.  
XO Pin Pull High : Enable RTD2168 embedded EDID.

## Mode Configure Table(Power On Latch)

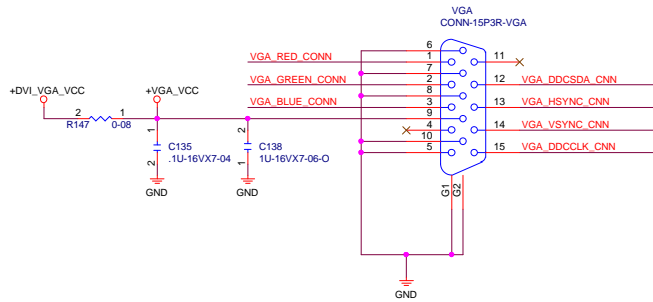
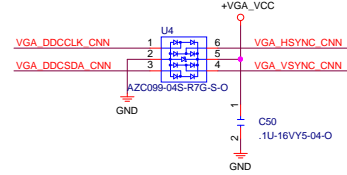
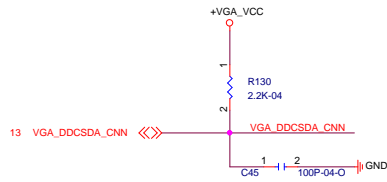
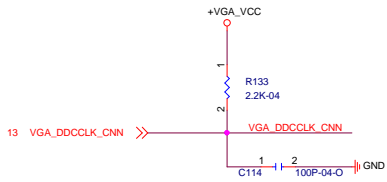
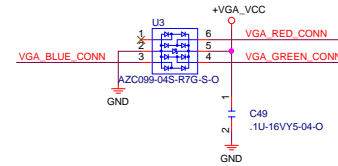
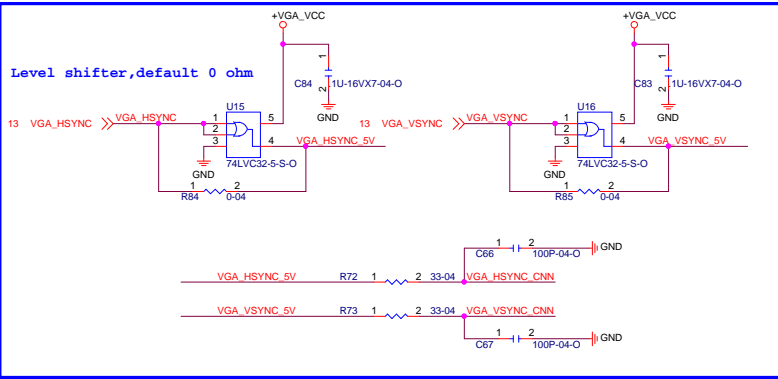
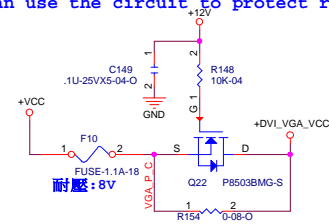
to set PIN22 pull low, PIN23 pull high for Rom mode.

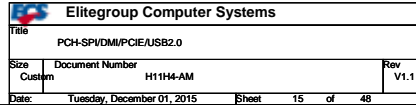


# VGA

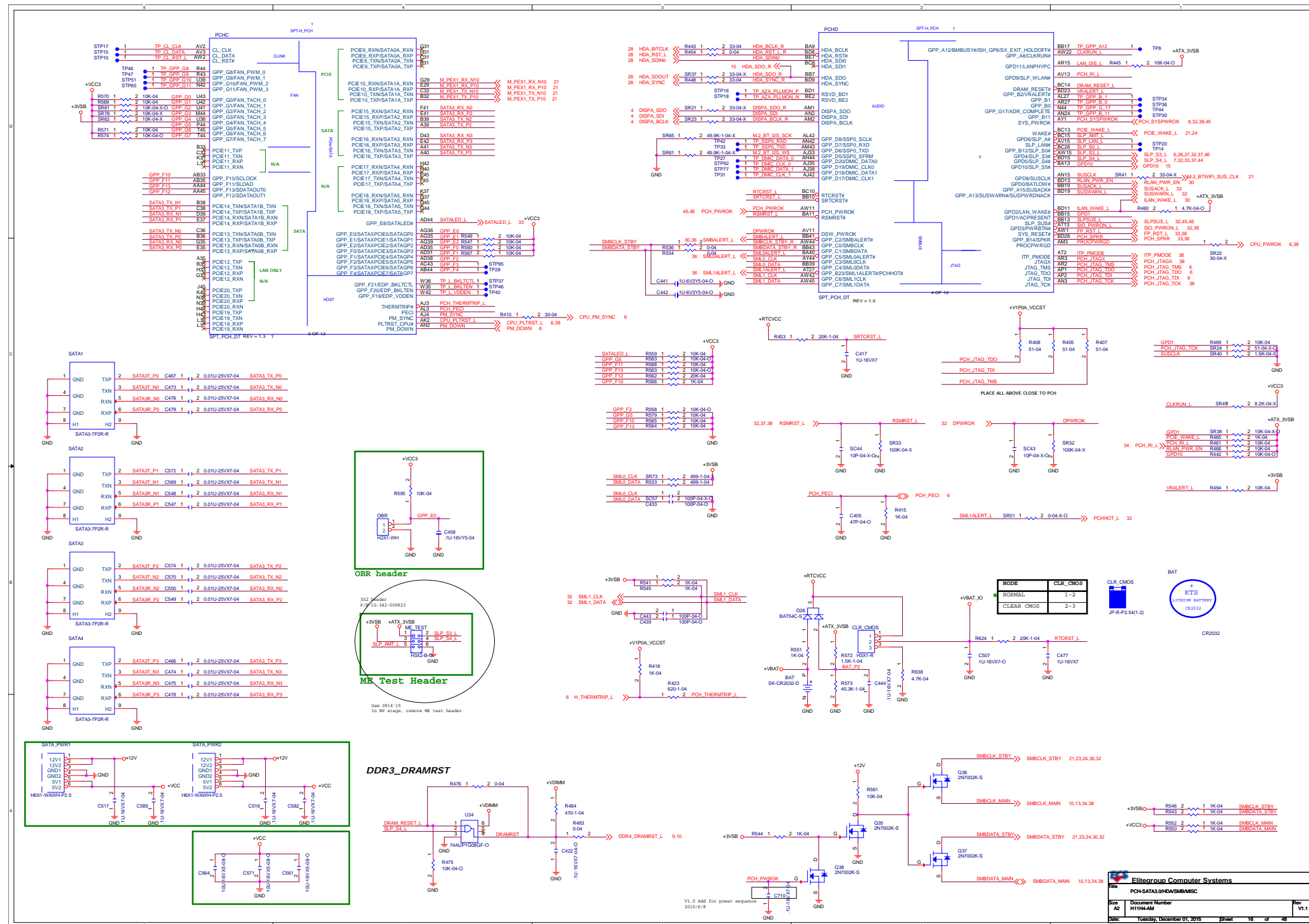


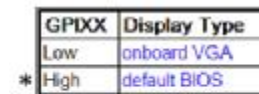
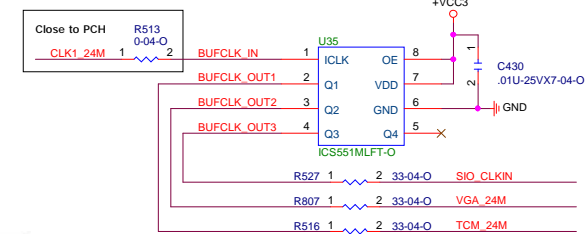
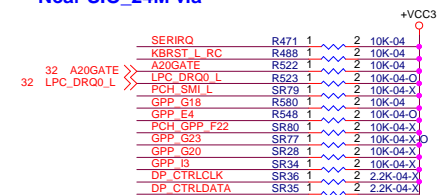
If build in Internal DVI Con,  
that can use the circuit to protect reverse voltage together.







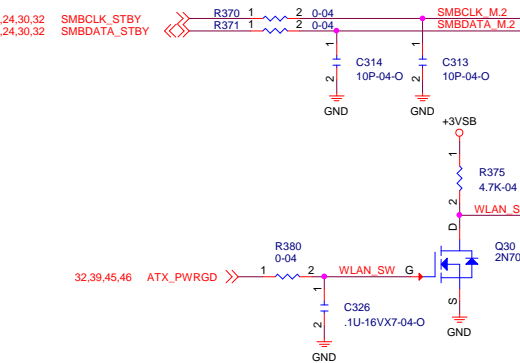
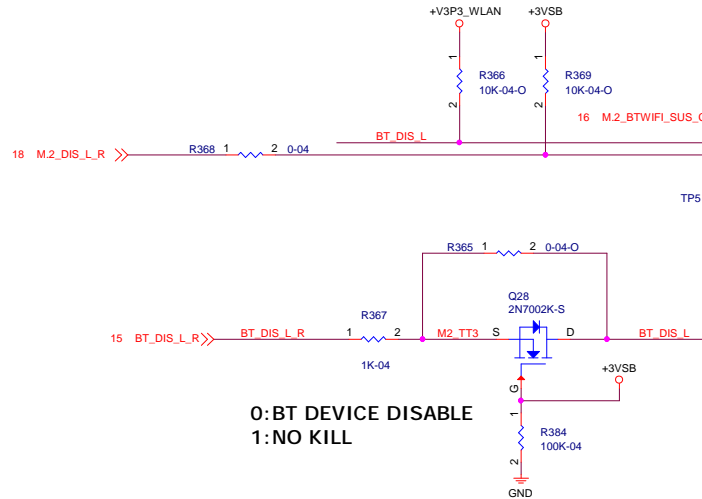




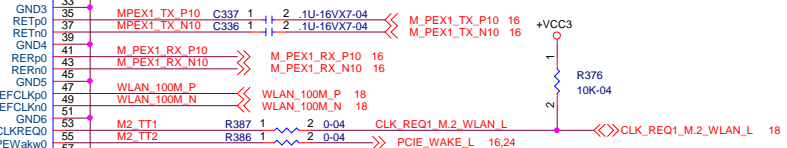
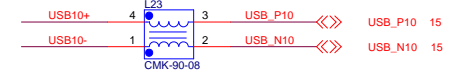
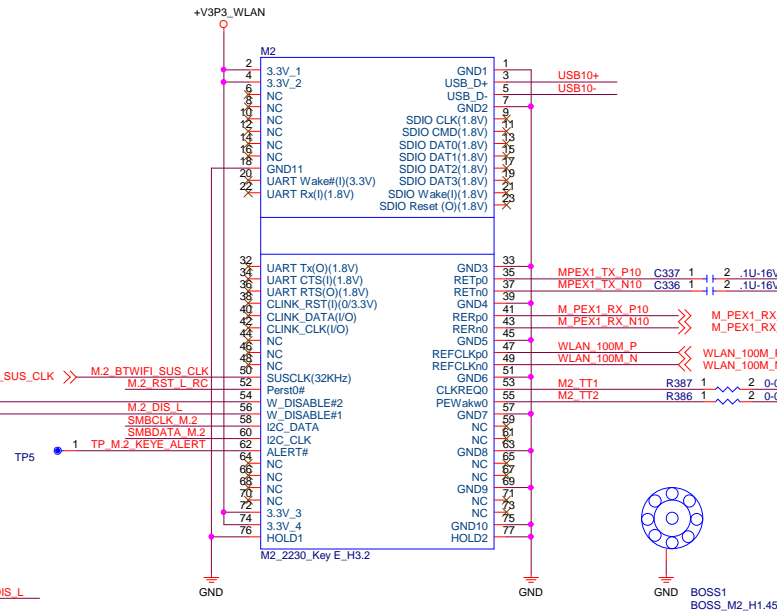




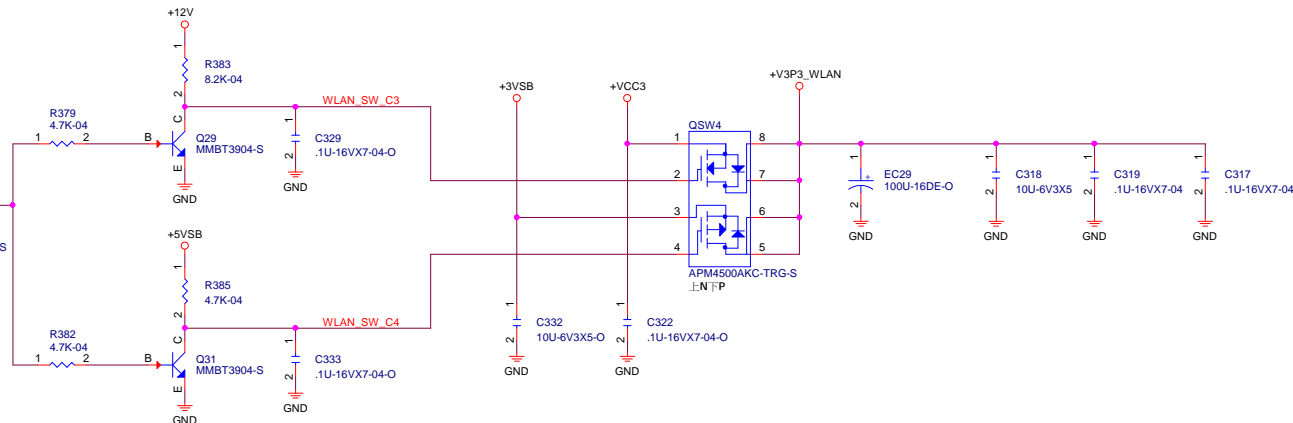


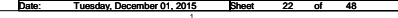


	ATX_PWRGD	+V3P3_WLAN
S0	1	+VCC3
S3/S4/S5	0	+3VSB



Key	Power Rail	Voltage Tolerance	Current Consumption Limit	
			Peak mA Max Avg @ 100 $\mu$ s	Normal mA Max Avg @ 1 s
E	3.3 V	$\pm 5\%$	2000	



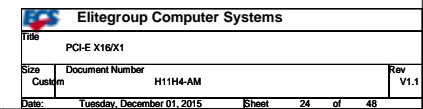




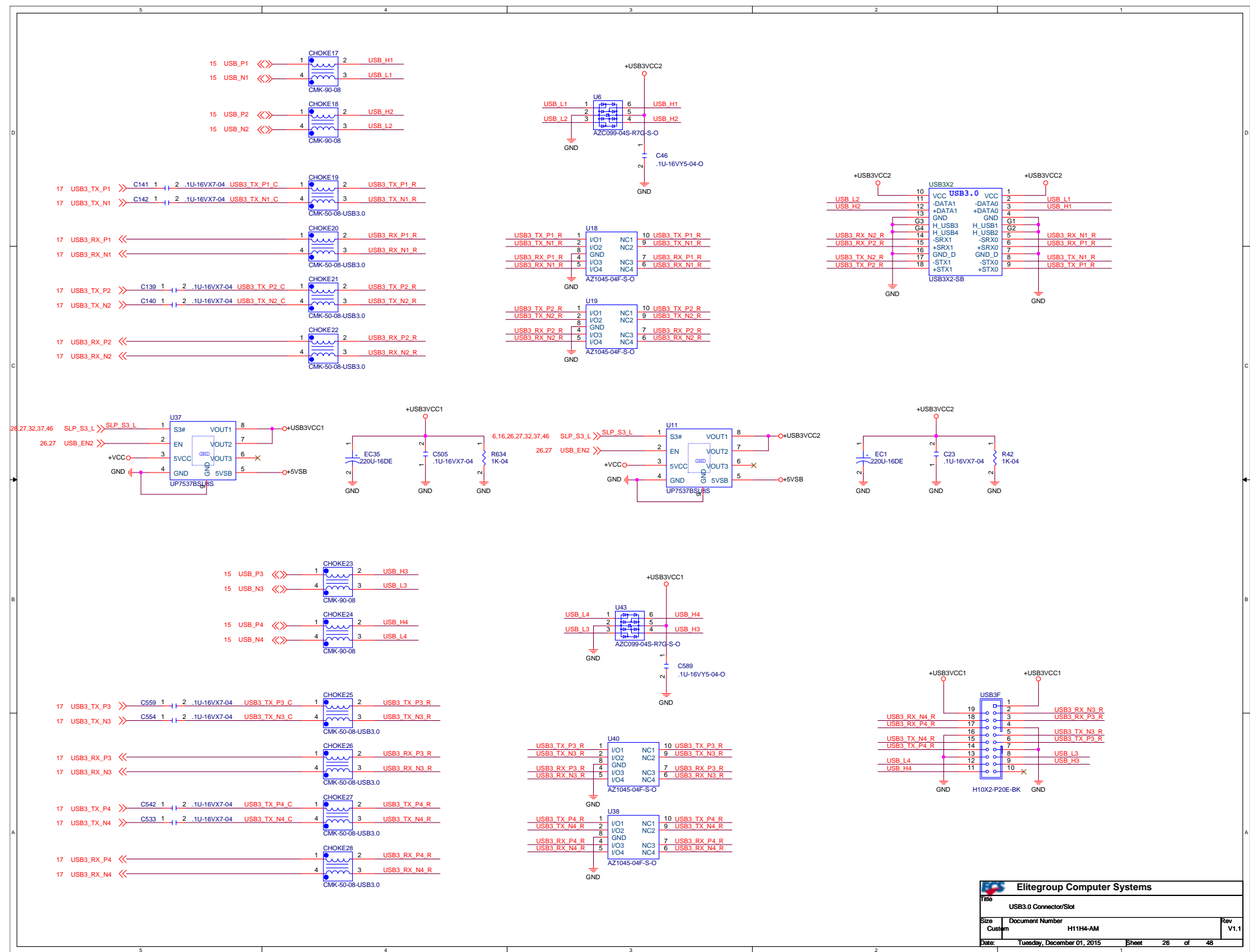


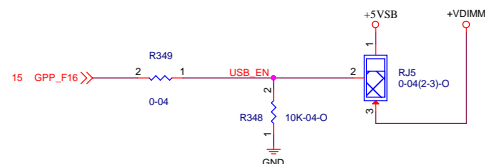
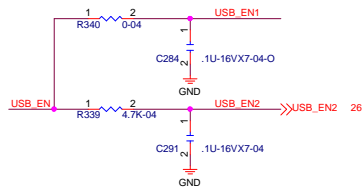
PCI-E X1 SLOT1

one slot support dual lan card, reserve

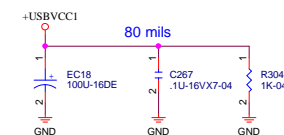
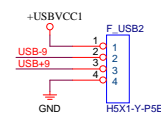
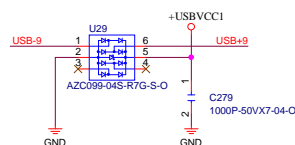
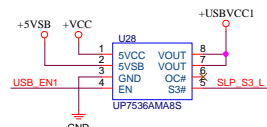
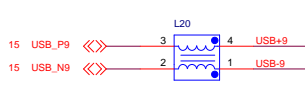




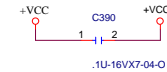
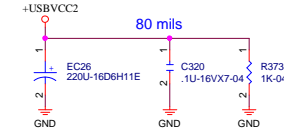
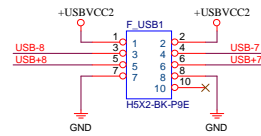
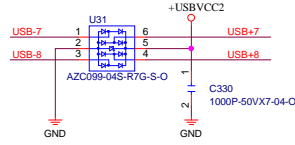
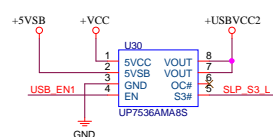
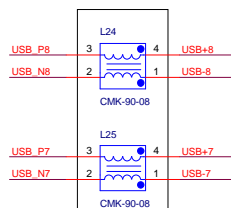




uP7536 Enable use	RJ?	RJ?	S4/S5 USB_5V_DUAL	Customer
VDIMM	0ohm (1-2)	NA	0 Volt	Acer S4 w/o S5 w/ USB_5VDUAL
5VSB	0ohm (2-3)	NA	5 Volt	
* GPIO	NA	0 ohm	S4 : 0 Volt S5 : 5 Volt	

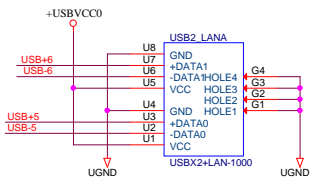
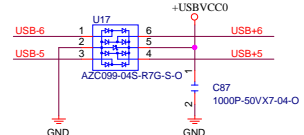
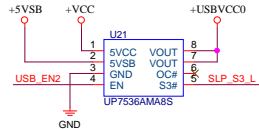
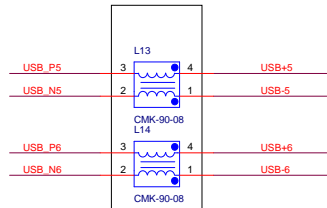
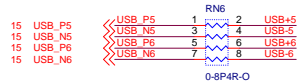


6,16,26,32,37,46 SLP\_S3\_L SLP\_S3\_L

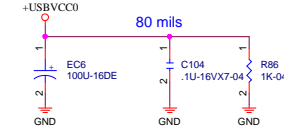


## USB2.0 header

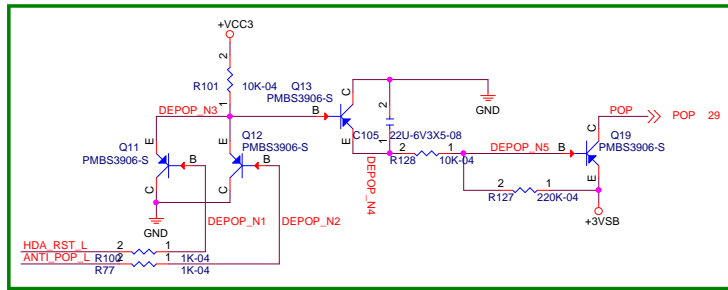
## USB2.0 connector



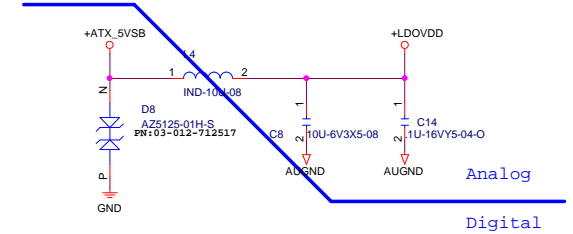
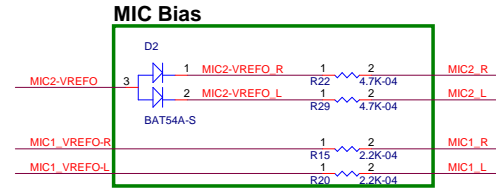
Lan + USB2.0



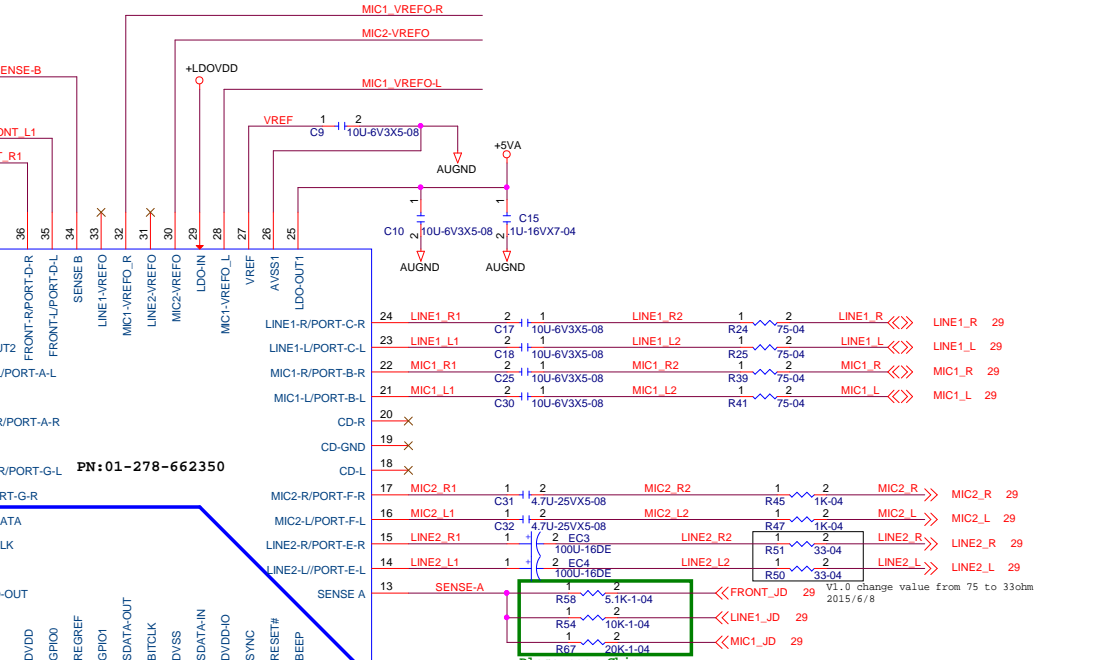
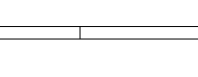
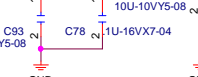
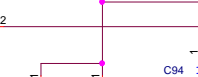
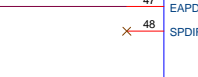
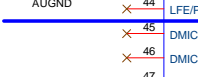
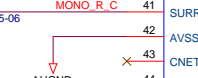
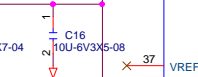
Elitegroup Computer Systems			
Title USB2.0 Connector/Header			
Size Custom	Document Number H11H4-AM		Rev V1.1
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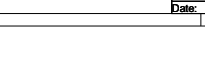
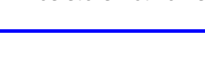
De-pop circuit



### Resistors Networks



### Resistors Networks




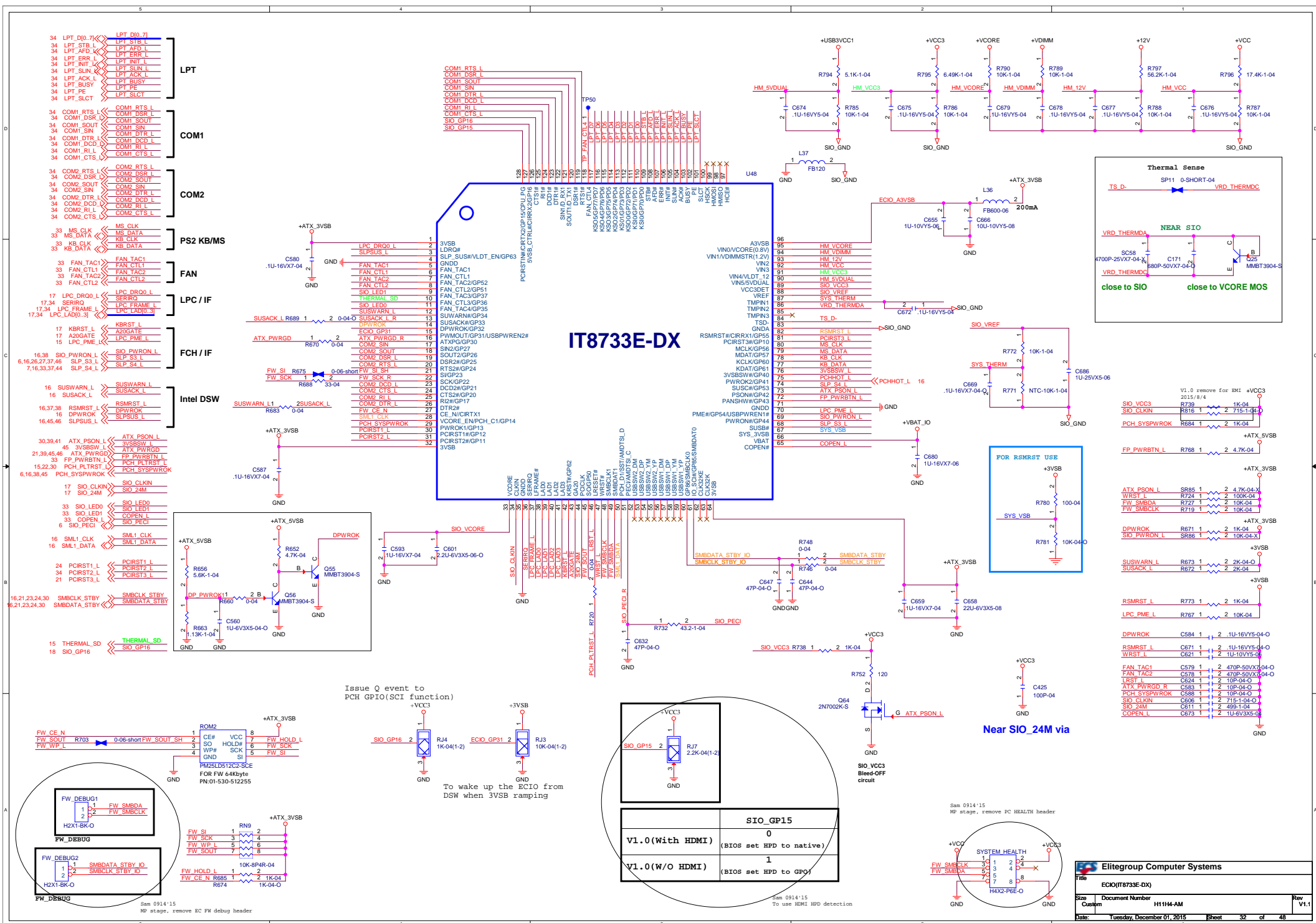
Elitegroup Computer Systems			
Title	Audio ALC662-VD		
Size	Document Number	H11H4-AM	Rev V1.1
Custom			
Date:	Tuesday, December 01, 2015	Sheet	28 of 48



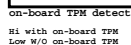


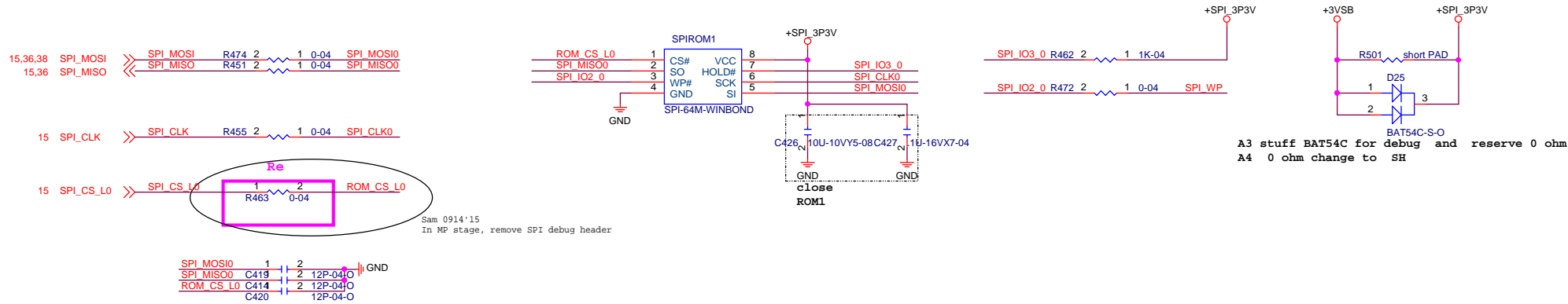


 Elitegroup Computer Systems				
Title Reserved				
Size Custom	Document Number H11H4-AM			Rev V1.1
Date:	Tuesday, December 01, 2015	Sheet	31	of 48

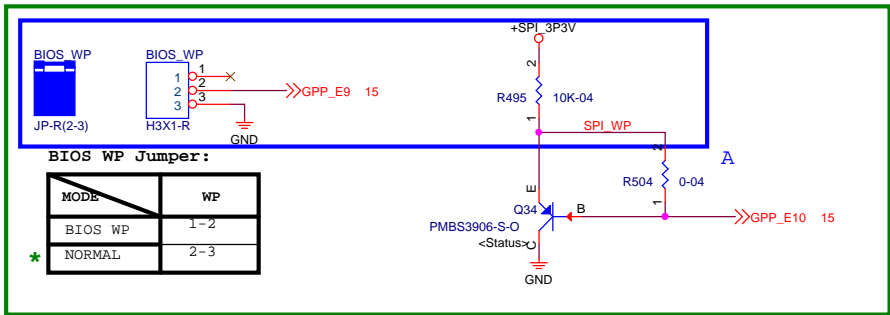




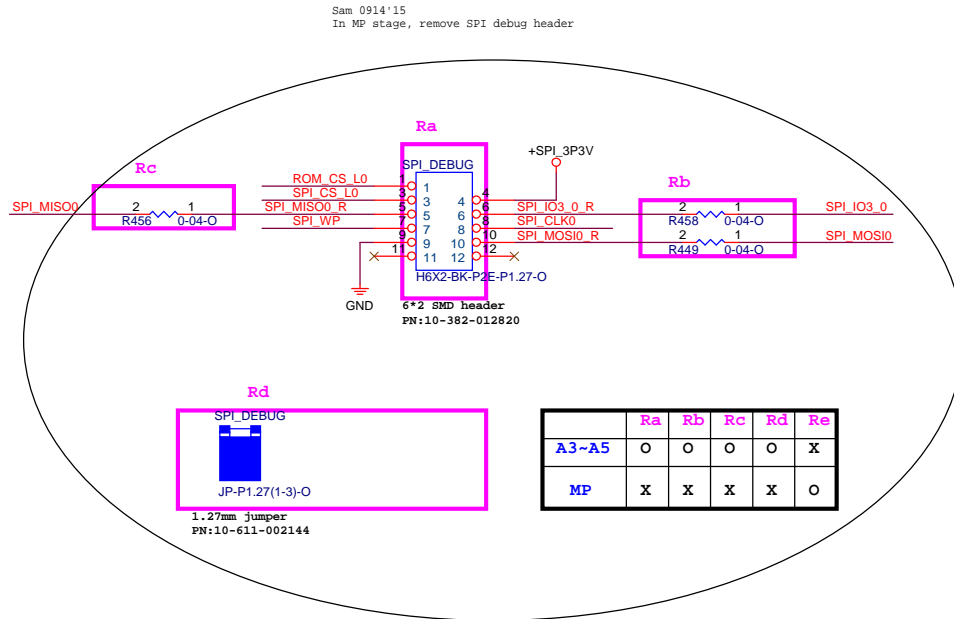


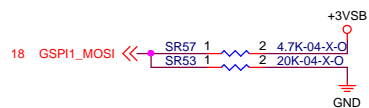


## SPI ROM

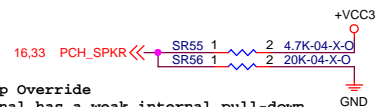


## BIOS WP

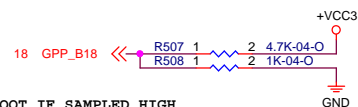




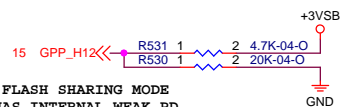
BOOT SELECT STRAP  
IF SAMPLED HIGH, LPC IS SELECTED ELSE SPI  
PCH HAS INTERNAL WEAK PD



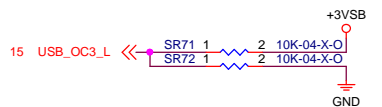
Top Swap Override  
The signal has a weak internal pull-down.  
0 = Disable "Top Swap" mode. (Default)  
1 = Enable "Top Swap" mode.



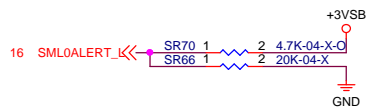
NO REBOOT IF SAMPLED HIGH  
PCH HAS INTERNAL WEAK PD



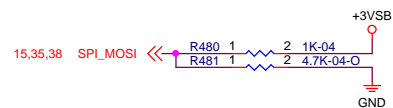
ESPI FLASH SHARING MODE  
PCH HAS INTERNAL WEAK PD  
0: MASTER ATTACHED FLASH SHARING  
1: SLAVE ATTACHED FLASH SHARING



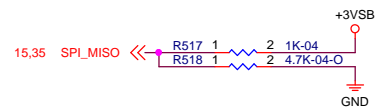
DFX TEST MODE  
XTAL INPUT IS SINGLE ENDED IF SAMPLED LOW ELSE DIFFERENTIAL



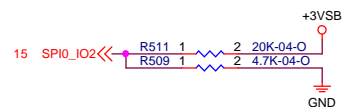
ESPI/LPC SELECT STRAP  
IF SAMPLED HIGH, ESPI IS SELECTED ELSE LPC  
PCH HAS INTERNAL WEAK PD



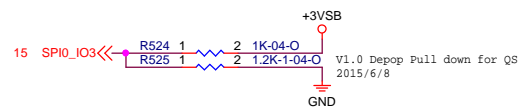
BOOT HALT ENABLED IF LOW  
PCH HAS INTERNAL WEAK PU



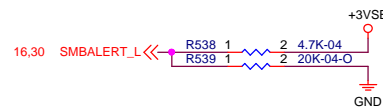
JTAG ODT IS DISABLED IF LOW  
PCH HAS INTERNAL WEAK PU



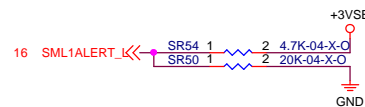
CONSENT STRAP IS ENABLED IF LOW  
PCH HAS INTERNAL WEAK PU



PERSONALITY STRAP IS ENABLED IF LOW  
PCH HAS INTERNAL WEAK PU  
(P.S. Pull down for pre ES1/ES1/ES2 only)



TLS CONFIDENTIALITY ENABLED  
IF SAMPLED HIGH(DEFAULT)  
PCH HAS INTERNAL WEAK PD

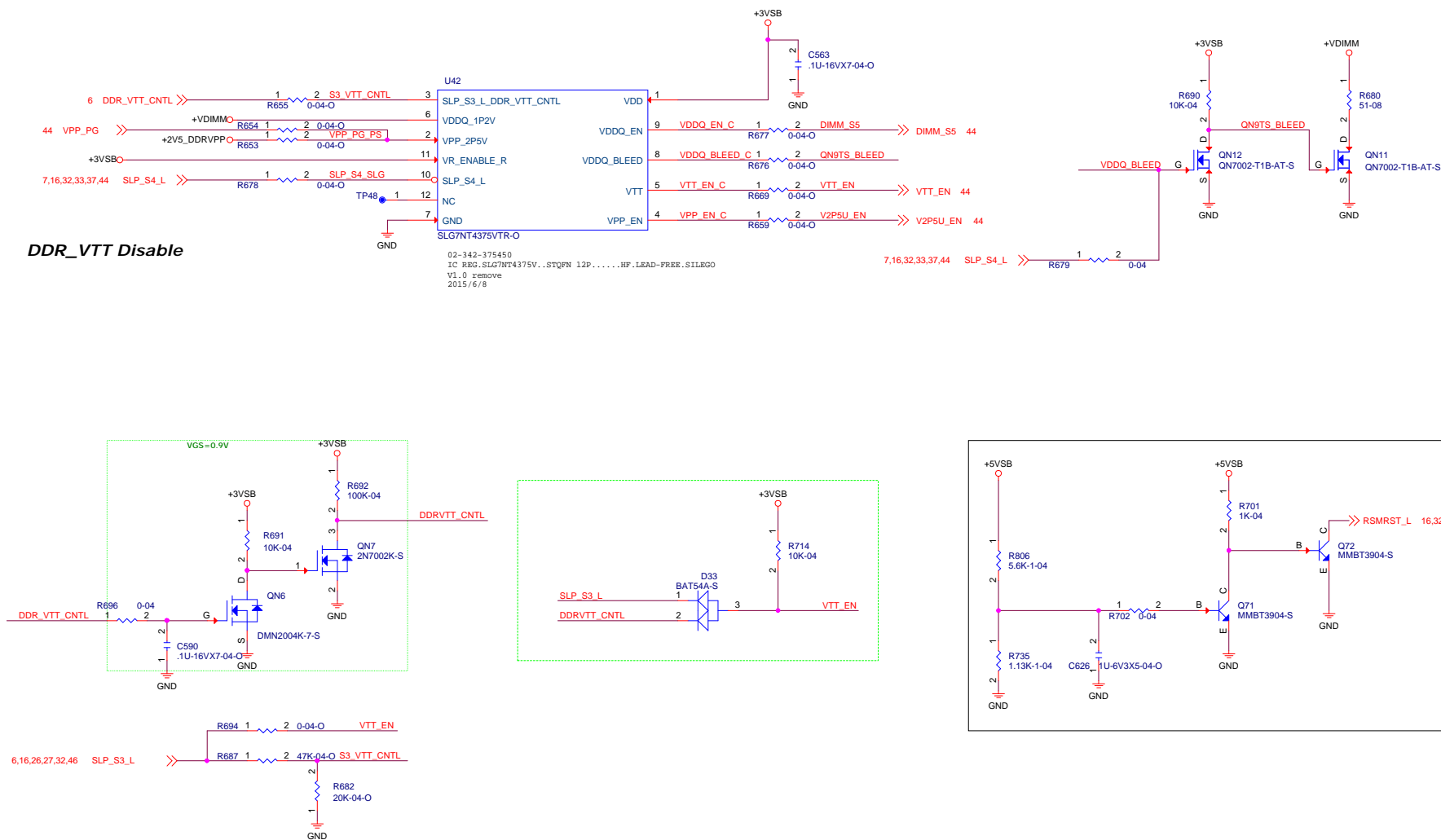


EXI BOOT STALL BYPASS IS ENABLED IF SAMPLED HIGH  
PCH HAS INTERNAL WEAK PD

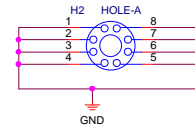
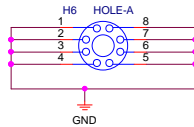
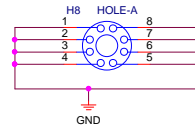
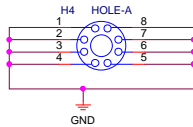
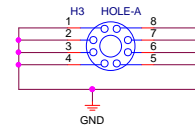
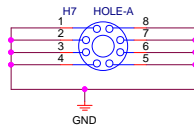
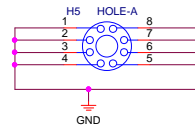
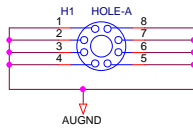
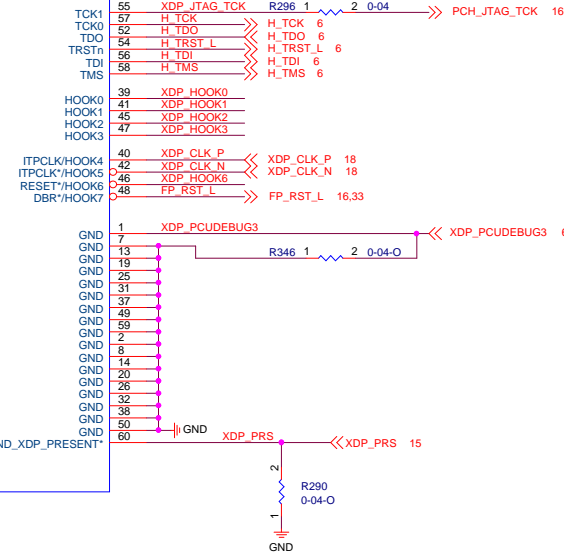
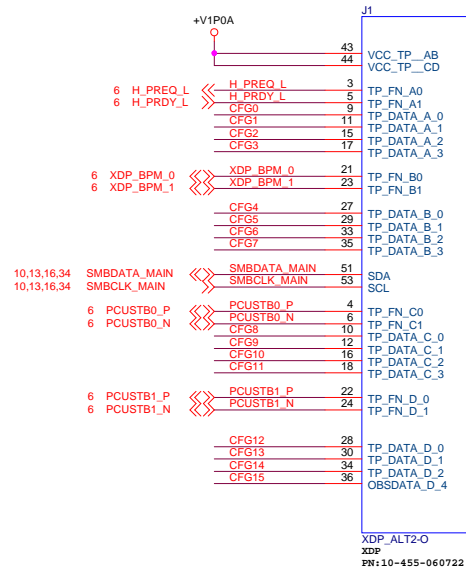
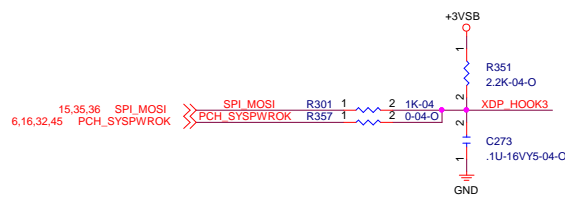
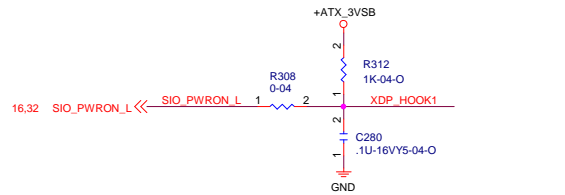
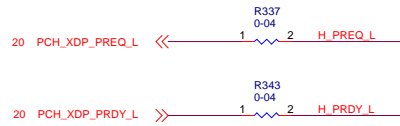
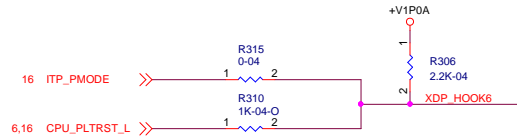
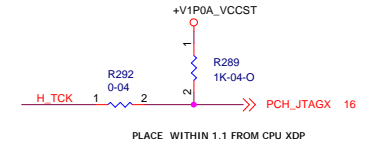
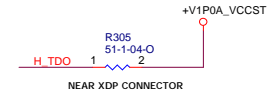
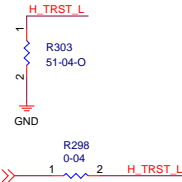
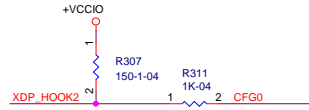
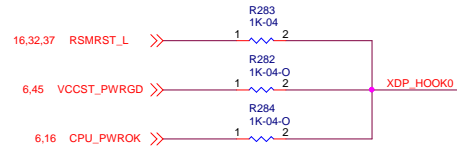
Title			Strap Pin
Size	Document Number	H11H4-AM	
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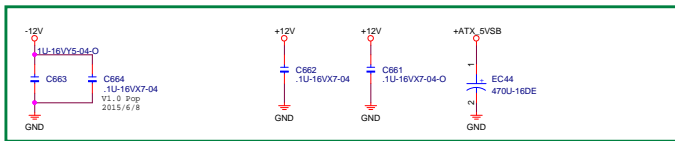
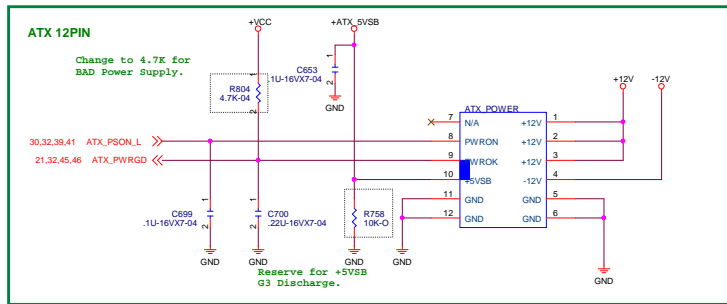
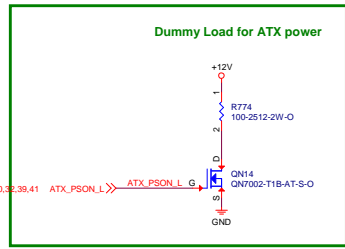
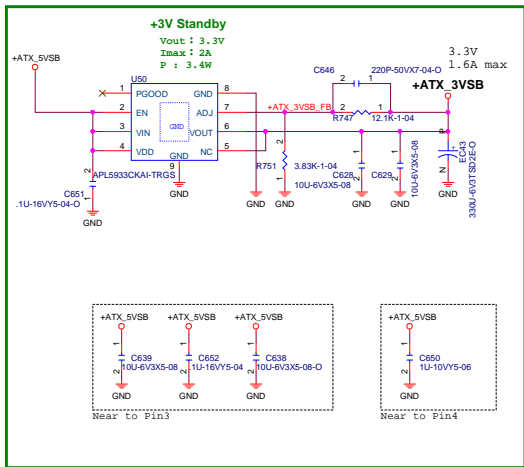
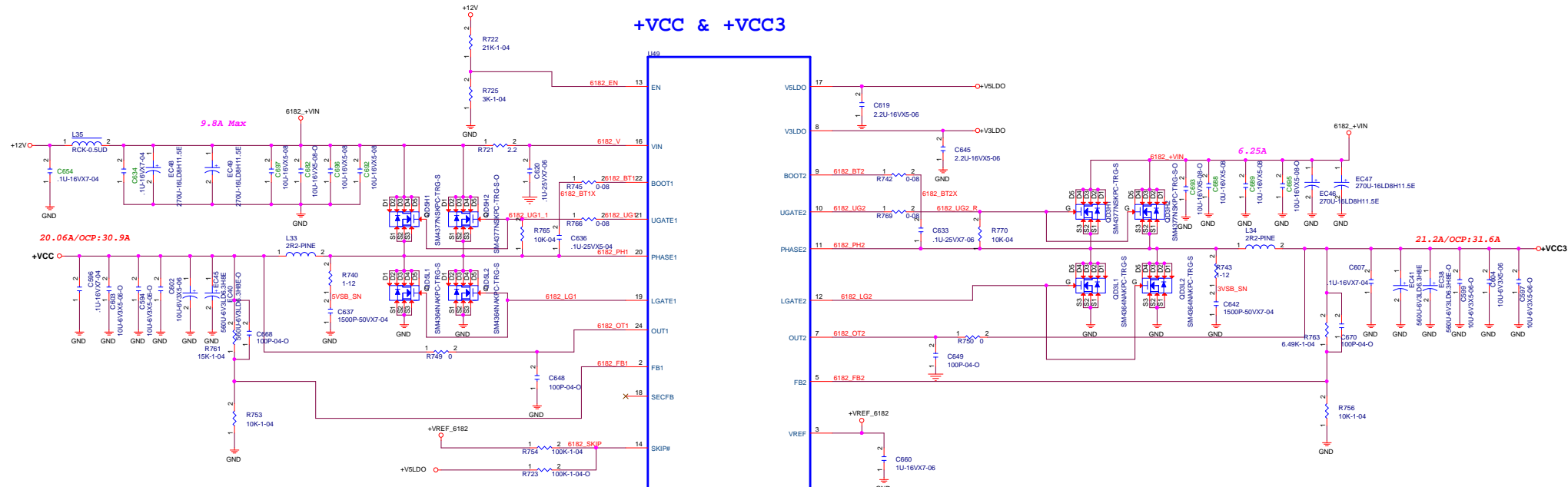
# DDR\_VTT Disable



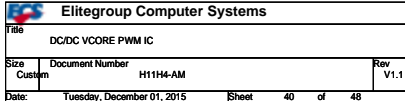
PLACE TRST\* TERMINATION ANYWHERE ON ROUTE.

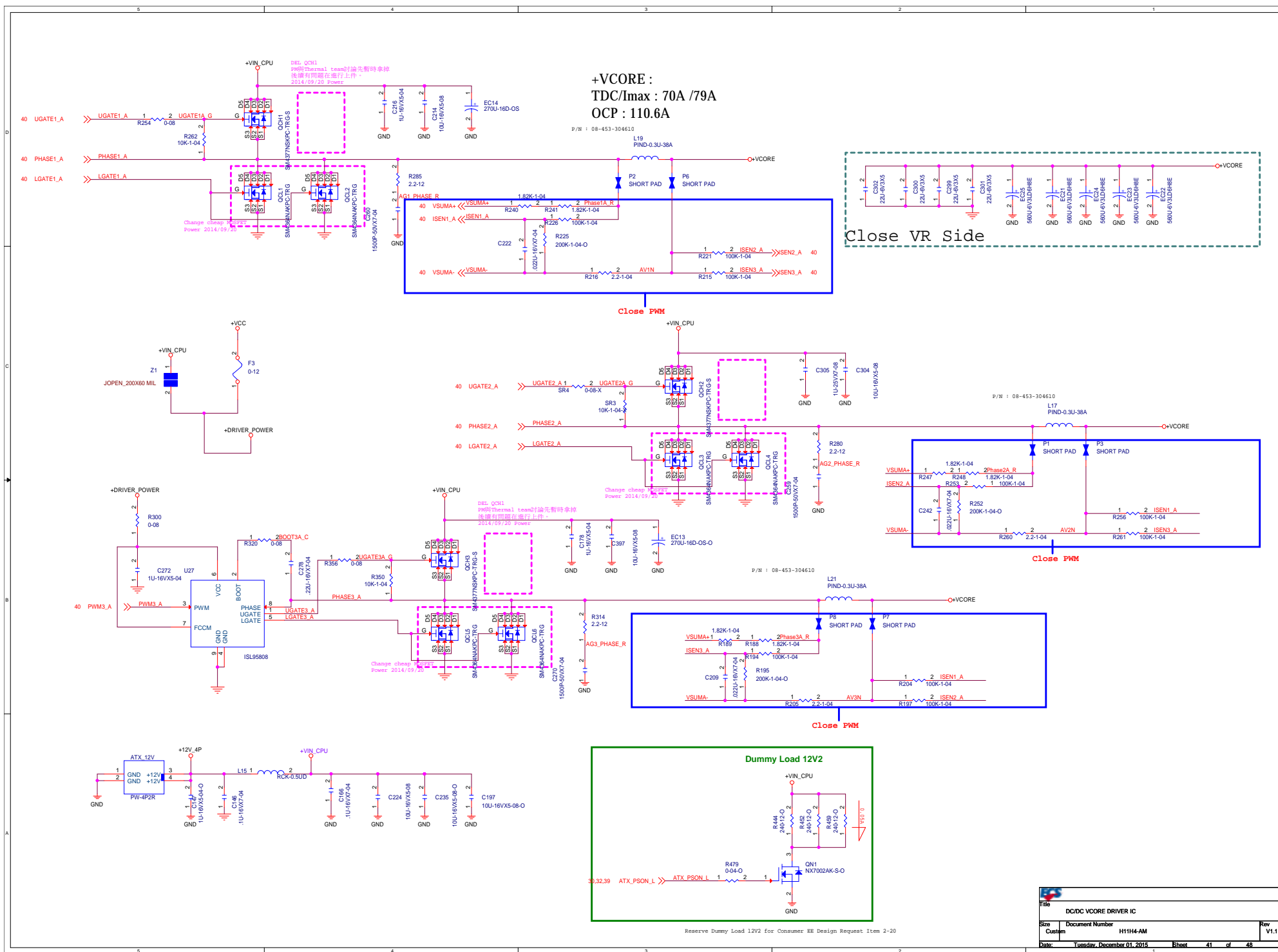


# +VCC & +VCC3

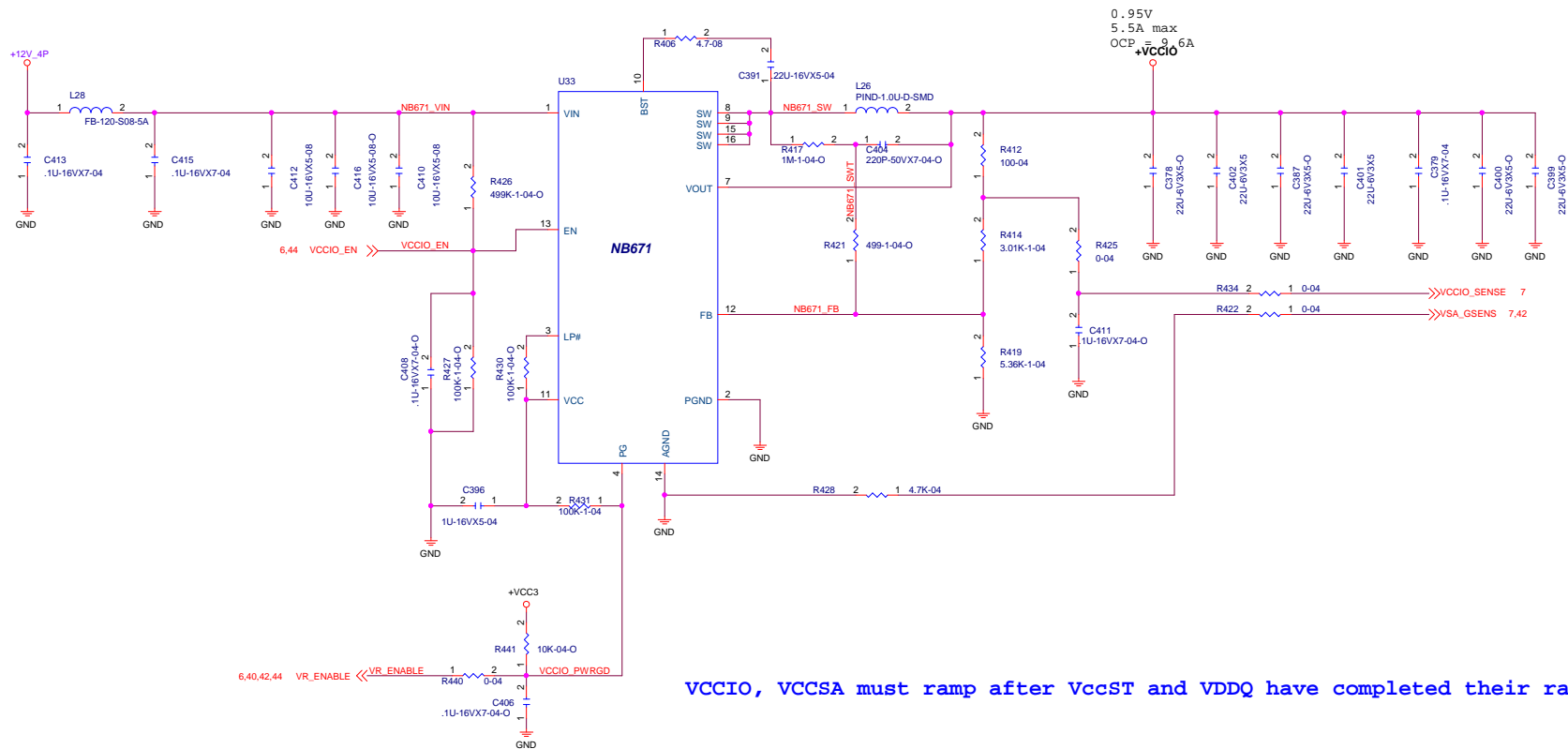


Elitegroup Computer Systems			
Title	+VCC AND +VCC3		
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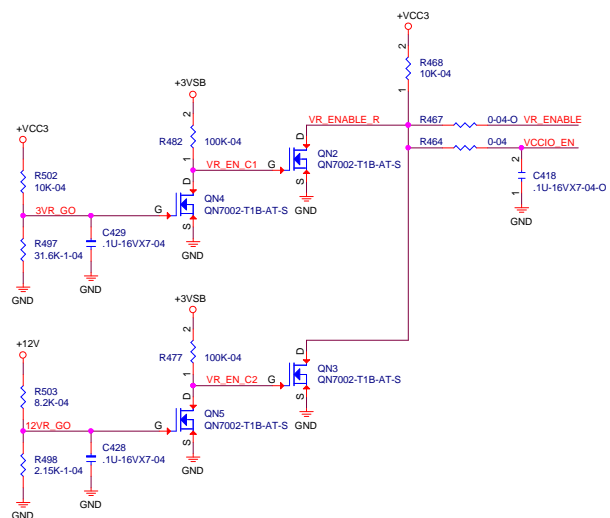






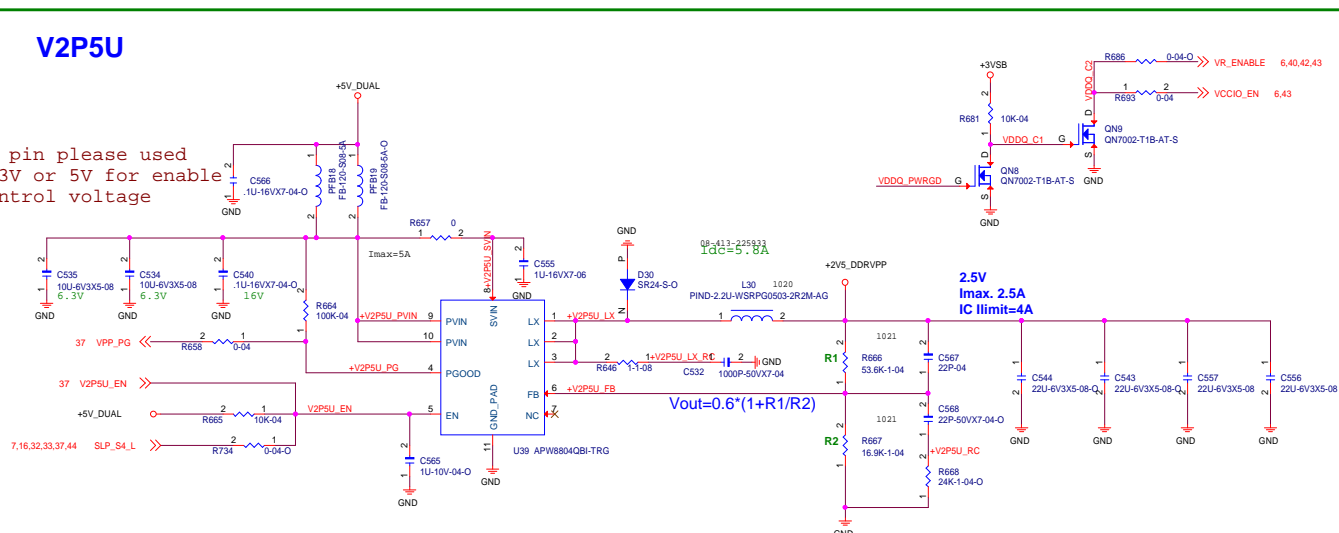


### VCCIO & VR ENABLE



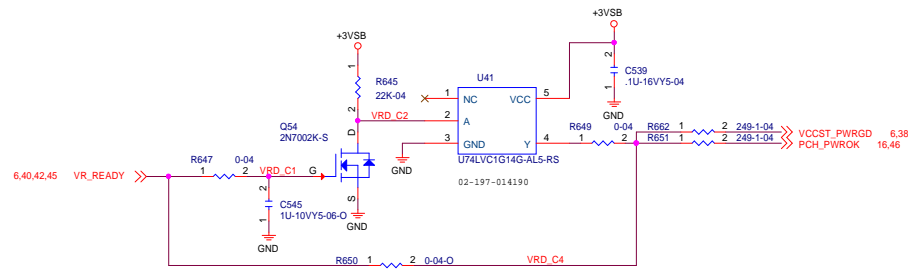
Title			
DC/DC VCCIO			
Size	Document Number	Rev	
Custom	H11H4-AM	V1.1	
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State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF

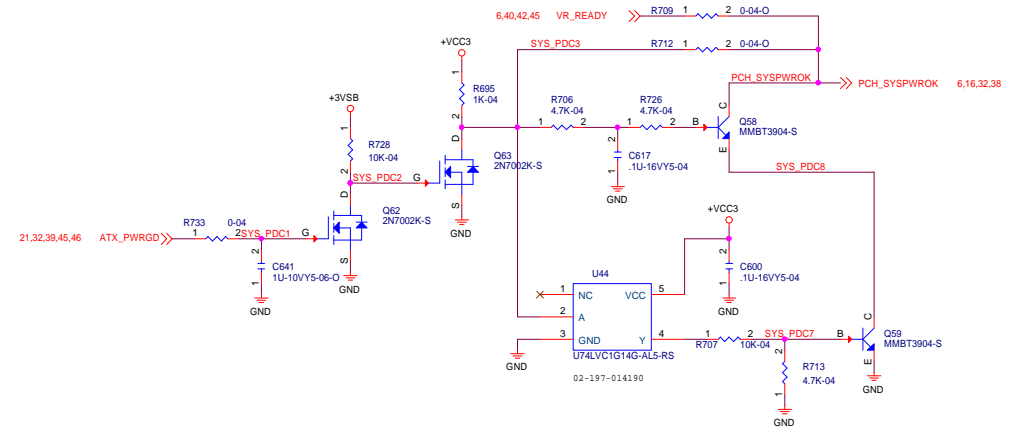




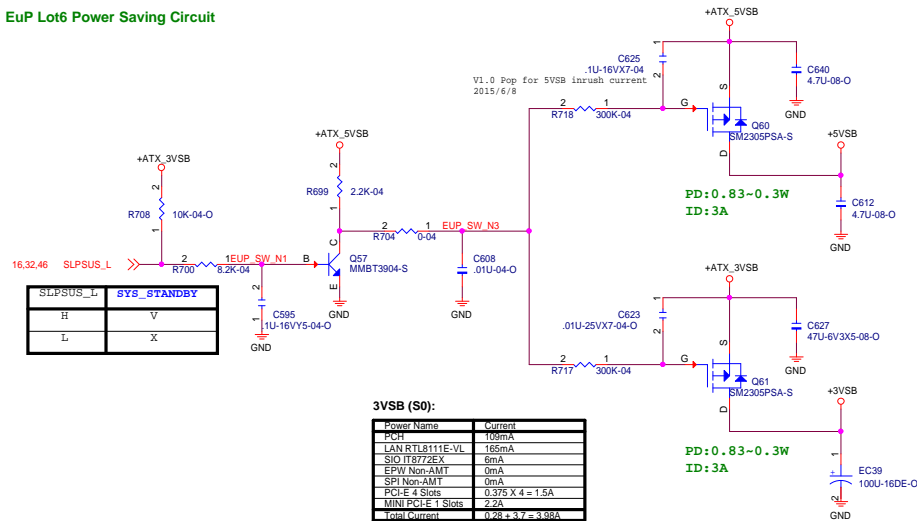
PCH & VCCST PWROK



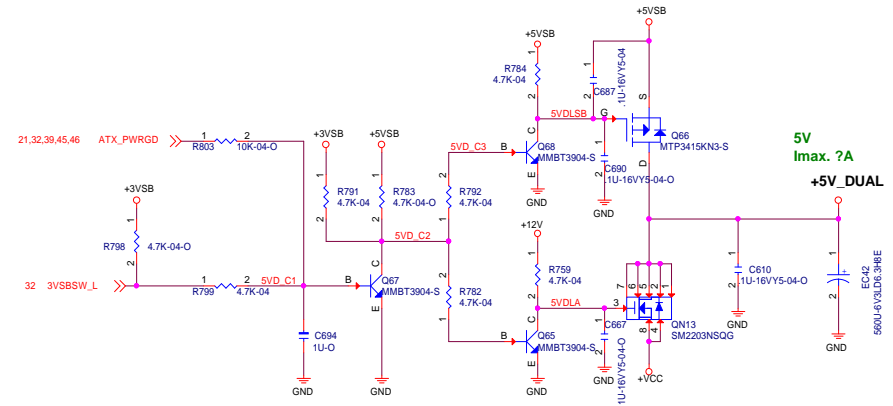
## SYS\_PWROK SURPRISE POWER DOWN TRIGGERED BY PWRGD\_PS




## EuP Lot6 Power Saving Circuit



## 5VDUAL

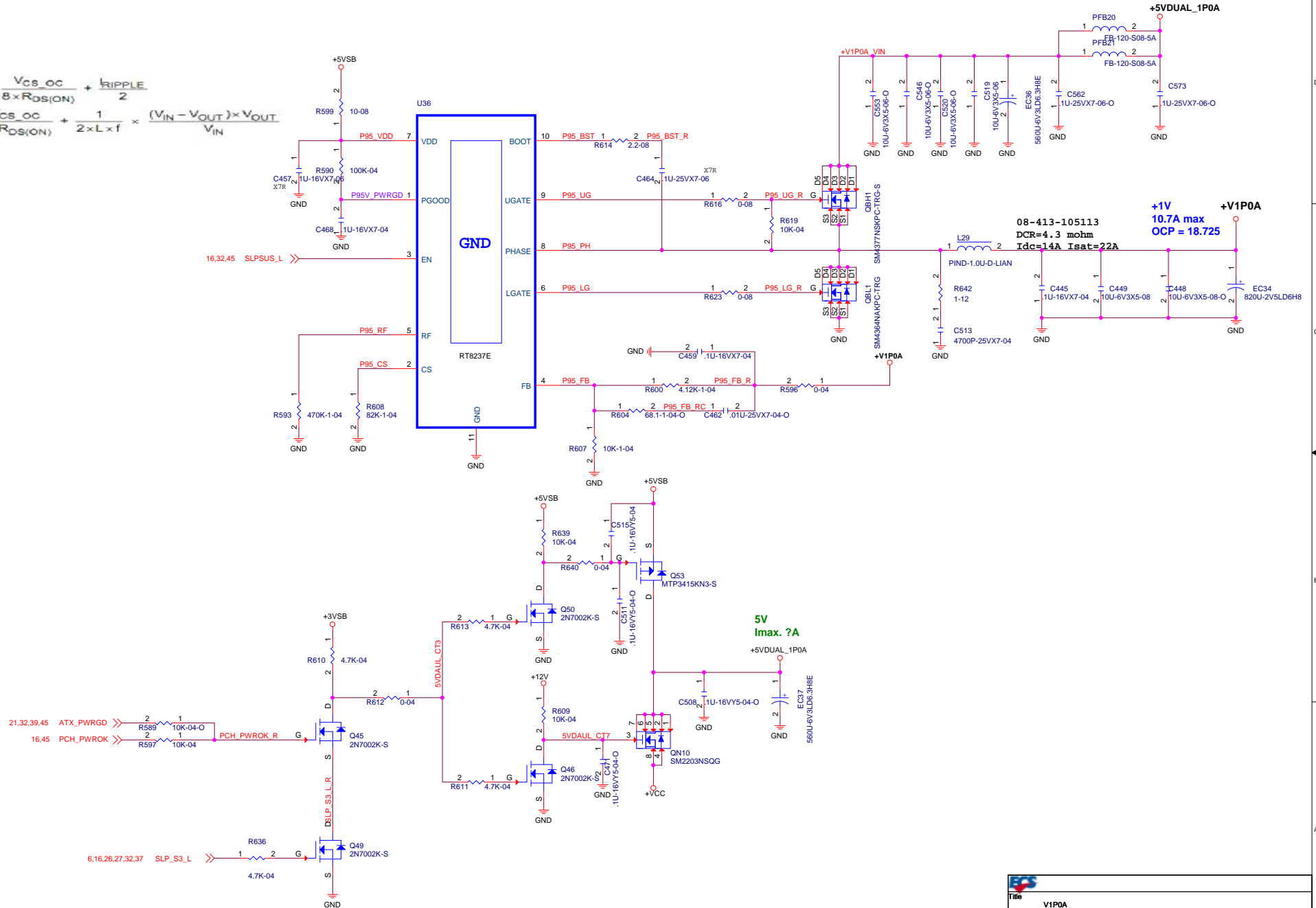


			
Title			
DC/DC DDRVPP & 5VDUAL			
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# V1P0A

$$I_{LOAD\_OC} = \frac{V_{CS\_OC}}{8 \times R_{DS(ON)}} + \frac{I_{RIPPLE}}{2}$$

$$= \frac{V_{CS\_OC}}{8 \times R_{DS(ON)}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$



Title			V1P0A
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Custom			
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